TiWi Transceiver Module

Audio Codec Application Note

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1 Introduction

1.1 Purpose & Scope

The purpose of this document is to provide details associated with the TiWi Bluetooth audio codec.

1.2 Audience

This document is intended to be read by engineers and technical management. A general knowledge of common engineering practices is assumed.

1.3 Applicable Documents

- *[1] TiWi Datasheet- LS240-WI-01-A20* (LSR)
- *[2] WL1271 Data Sheet: SWAS017V2.0, Texas Instruments, March 2009. Available only under NDA with Texas Instruments.*
- *[3] "Bluetooth (BL6450(L)/WL127x(L)/NL5500/WL128x) Vendor-Specific HCI Commands"- SWRU193G, Texas Instruments, September 2010.*

1.4 Revision History

Date	Change Description	Revision
1	Initial release.	0.0

Table 1 Revision History

2 Audio Codec

This application note describes the capabilities and operation of the TiWi modules audio codec. The module's audio codec interface is a direct breakout of the WL1271 audio codec [2].

2.1 Overview

The CODEC interface is a fully dedicated programmable serial port that provides the logic to interface toseveral kinds of PCM or I^2S codecs. The interface supports:

- Two voice channels
- Master / slave modes
- Coding schemes: u-Law, A-Law, Linear, Transparent
- Long & short frames
- Different data sizes, order and positions
- UDI profile
- High rate PCM interface for EDR
- Enlarged interface options to support a wider variety of Codecs
- PCM bus sharing

2.2 PCM Hardware Interface

The PCM interface is one implementation of the codec interface. It contains the following four lines:

- Clock--configurable direction (input or output)
- Frame Sync--configurable direction (input or output)
- Data In--Input
- Data Out--Output/Tri state

The WL1271 device can be either the master of the interface where it generates the clock and the frame-sync signals, or slave where it receives these two signals. The PCM interface is fully configured by means of a VS (Vendor Specific) command. Details about the command can be found in reference [3].

For slave mode, clock input frequencies of up to 16 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits. For master mode, the WL1271 can generate any clock frequency between 64 kHz and 4.096 MHz.

2.3 Data Format

The data format is fully configurable:

• The data length can be from 8 to 320 bits, in 1-bit increments, when working with two channels, or upto 640 bits when using 1 channel. The data length can be set independently for each channel.

• The data position within a frame is also configurable with 1-clock (bit) resolution, and can be set independently (relative to the edge of the Frame Sync signal) for each channel.

• The Data_In and Data_Out bit order can be configured independently. For example; Data_In can start with MSB while Data_Out starts with LSB. Each channel is separately configurable. The inverse bit order (i.e. LSB first) is supported only for sample sizes up to 24 bits.

• The data in and data out size do not necessarily have to be the same length.

• The Data_Out line is configured as a 'high-Z' output between data words. Data_Out can also be set for permanent high-Z, irrespective of data out. This allows the WL1271 to be a bus slave in a multi-slave PCM environment. At power up, Data_Out is configured as high-Z.

2.4 Frame Idle Period

The CODEC interface has the capability for frame-idle periods, where the PCM clock can "take a break" and become '0' at the end of the PCM frame, after all data has been transferred. Refer to Figure 1 below.

The WL1271 supports frame-idle periods both as master and slave of the PCM bus.

When WL1271 is the master of the interface, the frame-idle period is configurable. There are 2 configurable parameters:

• Clk_Idle_Start - Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock becomes '0'.

• Clk_Idle_End – Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of PCM clock periods. The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

For example, and for a PCM clock rate = 1 MHz, frame sync period = 10 kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90.

Between each two-frame sync pulses, there are 70 clock cycles (instead of 100). The clock idle period starts 60clock cycles after the beginning of the frame and lasts 90-60=30 clock cycles. This means that the idleperiod ends 100-90=10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.

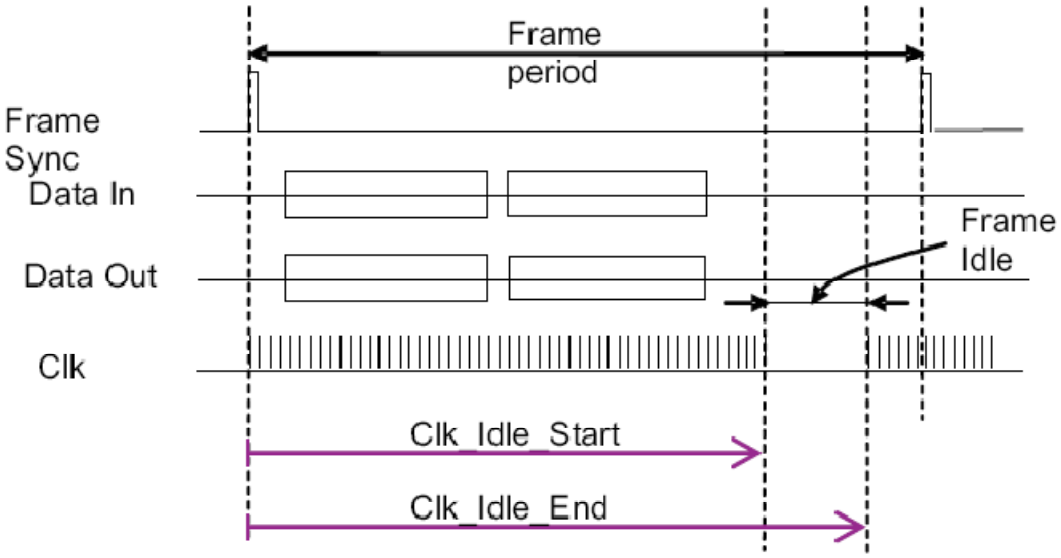

FIGURE 1: Frame timing description.

2.5 Clock Edge Operation

The CODEC interface of the WL1271 can work on the rising or the falling edge of the clock. It also has the ability to sample the frame sync and the data at inversed polarity.

The following diagram in Figure 2 shows the operation of a falling-edge-clock type of codec. The codec is the master of the PCM bus. The frame-sync signal is updated (by the codec) on the falling clock edge and therefore is sampled (by the WL1271) on the next rising clock. The data from the codec is sampled (by the WL1271) on the clock falling edge.

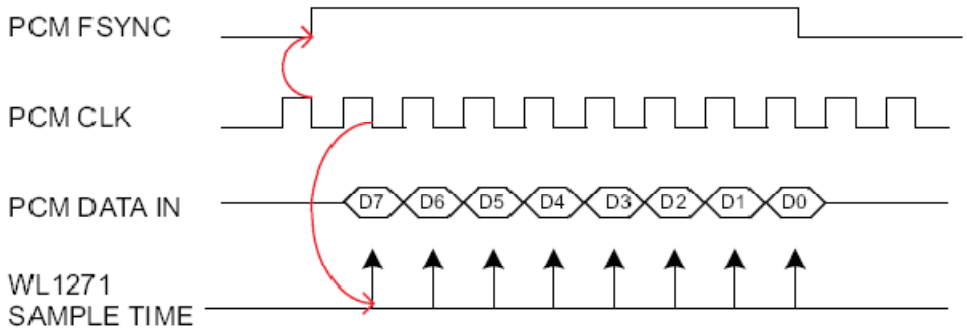

FIGURE 2: Negative Clock PCM Operation.

2.6 Two Channel PCM Bus Example

Presented in Figure 3 is a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame. (FT stands for Frame Timer).

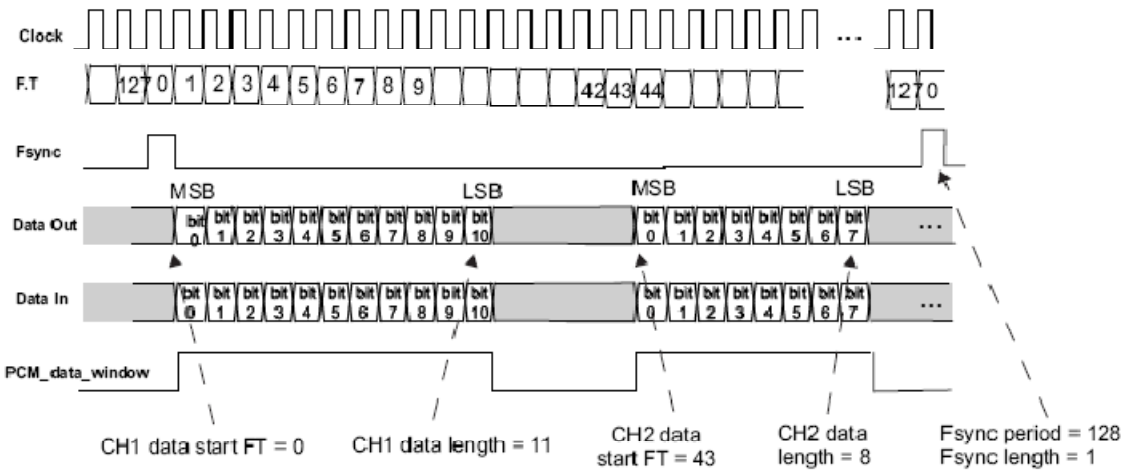

FIGURE 3: Two channel bus timing

2.7 Audio Encoding

The WL1271 CODEC interface can use one of four audio coding patterns:

- A-Law (8-bit)
- μ-Law (8-bit)
- Linear (8 or 16-bit)
- Transparent.

2.8 Improved Algorithm for Lost Packets

The WL1271 features an improved algorithm for improving voice quality when received voice data packets go missing. There are two options:

- Repeat the last sample – possible only for sample sizes up to 24 bits. For sample sizes >24 bits, the last byte is repeated.

- Repeat a configurable sample of 8-24 bits (depends on the real sample size), in order to simulate silence (or anything else) in the PCM bus. The configured sample is written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.

2.9 WL1271 BT Function PCM Clock Mismatch Handling

In the BT RX mode, the WL1271 receives RF voice packets and writes these to the CODEC I/F. If the WL1271receives data faster than the CODEC I/F output allows, an overflow occurs. In this case, the WL1271 BT function has 2 possible behavior modes: ‘allow overflow’ and ‘don’t allow overflow’.

- If overflow is allowed, the WL1271 BT function continues receiving data and overwrites any data not yet sent to the CODEC.

- If overflow is not allowed, RF voice packets received when buffer is full, are discarded.

2.10 WL1271 Bluetooth I²S Interface

The WL1271 can be configured as a Inter-IC Sound (I²S) serial interface to a I²S CODEC device. In this mode, the WL1271 audio CODEC interface is configured as a bi-directional, full duplex interface, with two time slots per frame: Time slot 0 is used for the left channel audio data and time slot 1 for the right channel audio data. Each time slot is configurable up to 40 serial clock cycles in length and the frame isconfigurable up to 80 serial clock cycles in length.

3 Contacting LS Research

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