# TiWi Family Application Guide


Last updated
February 11, 2016

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# 1 Introduction

## 1.1 Purpose & Scope

The purpose of this document is to provide application guidance in the integration of a TiWi-R2, TiWi-BLE, or TiWi5 module into a product design.

## 1.2 Applicable Documents

- *TiWi-R2 Datasheet*
- *TiWi-BLE Datasheet*
- *TiWi5 Datasheet*
- *Texas Instruments Application Report SCEA043*
  *http://focus.ti.com/lit/an/scea043/scea043.pdf*
- *Texas Instruments Application Report SCEA044*
  *http://focus.ti.com/lit/an/scea044/scea044.pdf*
- *Texas Instruments Voltage Level Translation Selections*
  *http://focus.ti.com/download/aap/pdf/VLT_PF_Overview.pdf*

## 1.3 Revision History

| Date | Change Description | Revision |
|---|---|---|
| 9-26-2011 | Initial release. | 1.0 |
| 6-11-2012 | Changed to application guide for TiWi-R2, BLE and 5. | 1.1 |
| 10-02-2014 | Made separate sections for TiWi-R2/BLE & TiWi5 | 1.2 |
| | | |

**Table 1 Revision History**

# 2 TiWi SDIO Buffer Behavior

## 2.1 SDIO_D3

When operating as a digital output, SDIO_D3 does not require a SDIO Controller (or level shifter) capable of pulling the line high for TiWi. Within the TiWi module, SDIO_D3 is equipped with approximately 3.21k pull up resistance, while all other SDIO I/O are not pulled up.

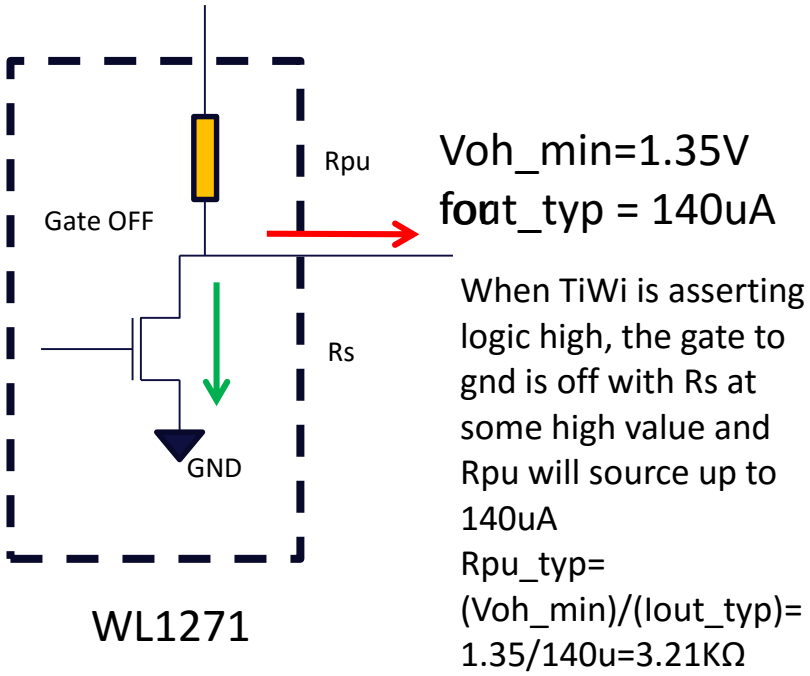



**Figure 1 Logic High: TiWi SDIO_D3**

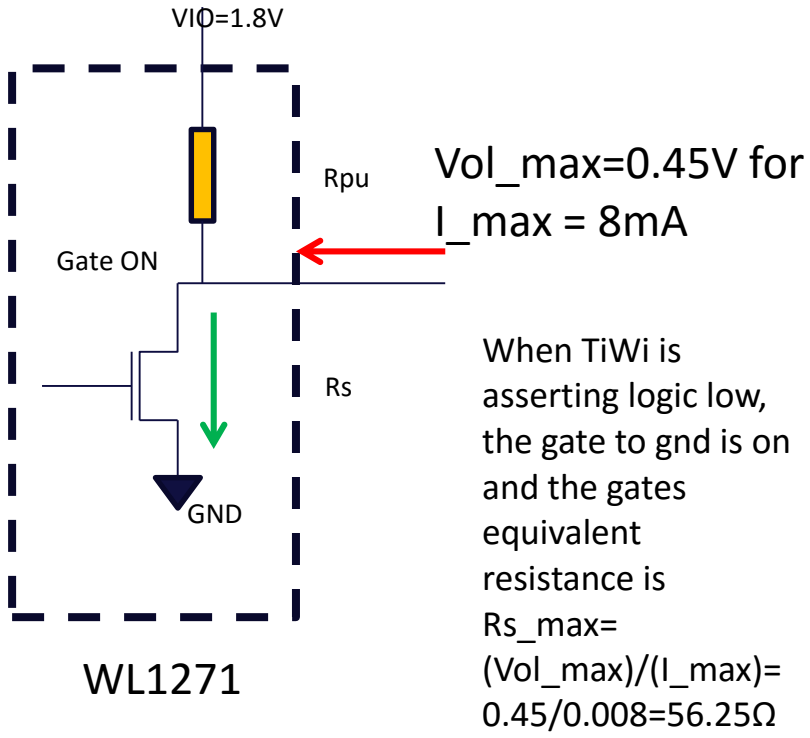



**Figure 2 Logic Low: TiWi SDIO_D3**

## 2.2 All SDIO I/O Except SDIO_D3

All of the SDIO I/O, *except* SDIO_D3, require a SDIO Host Controller (or level shifter) capable of pulling the line high for TiWi. An external pull up resistor may be used, but the particular circuit would require detailed analysis to choose the correct value without violating the logic voltage thresholds. The added resistor or network would need to support the data rates and analog rise and fall time of the SDIO bus. Ω

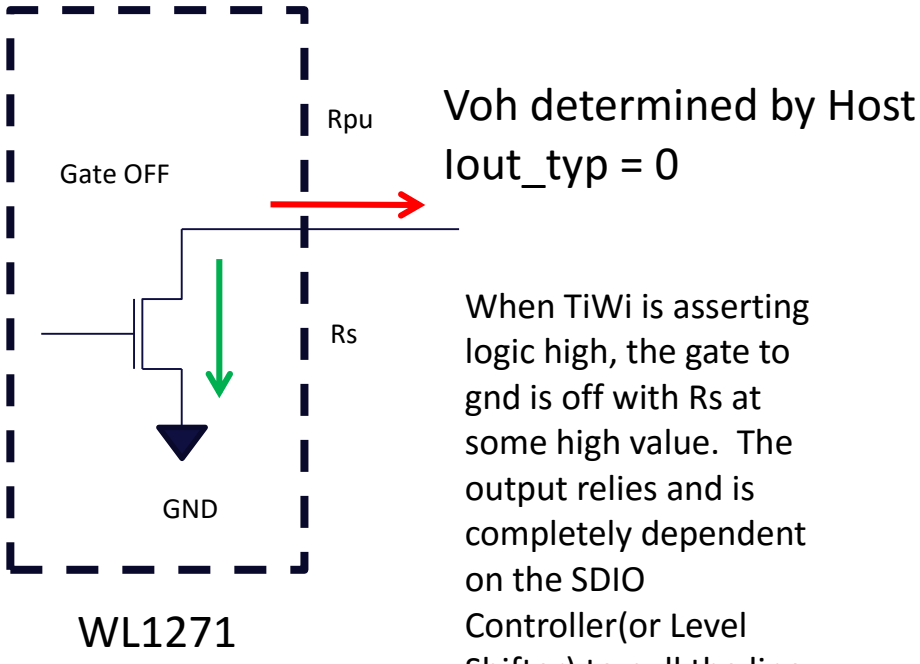



**Figure 3 Logic High: All TiWi SDIO Except SDIO_D3 (open drain requires pull up)**

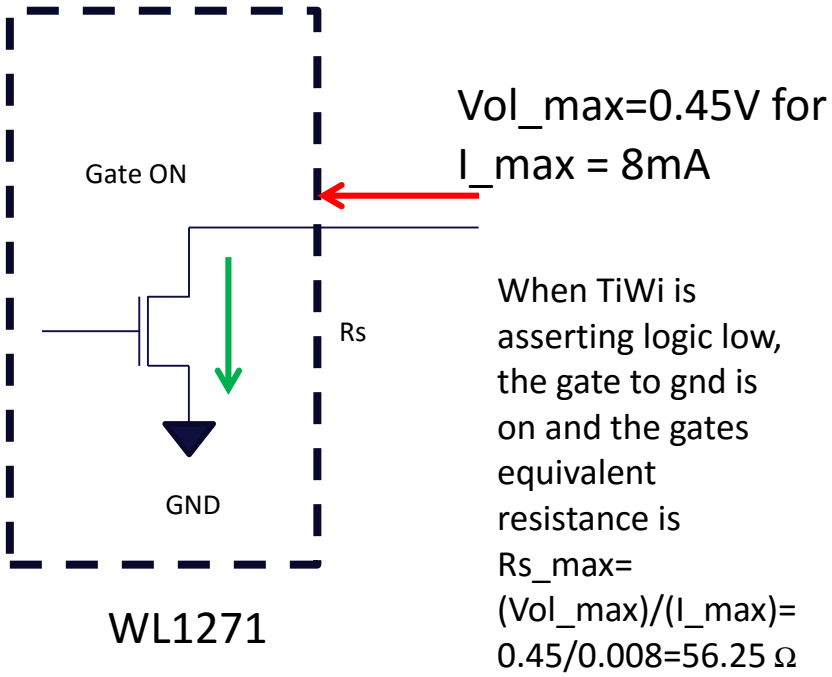



**Figure 4 Logic Low: All TiWi SDIO Except SDIO_D3 (open drain requires pull up)**

# 3 SDIO Level Shifter Considerations

## 3.1 Texas Instruments TXB010x Type Voltage Translators

Below is a snapshot of the architecture of the Texas Instruments TXB010x type voltage translators. Notice the SDIO signal to be level translated passes between the A and B ports, and neither port has an internal pull up resistance. Since all SDIO lines except for D3 require an external pull up resistance, this is an option only for SDIO_D3 which already has the pull up inside the TiWi module. The appropriate one-shot fires briefly for edge acceleration, then the buffer with series 4K Ω takes over. This would likely not work since when driving a logic low, the 4K Ω is in series with the 3.21K Ω within the TiWi module. This voltage divider results in 0.99 V presented to the TiWi module as a logic low. While this does not meet TiWi's Vil_max requirement of 0.63V, we are close and considering the silicon process variation, **this would work intermittently at best, but likely not at all.** It may work with an external pull up network, but there are other choices which will work for all SDIO lines including D3. We suggest detailed analysis of the capabilities of the SDIO Master (or level shifter) and how it relates to and is affected by the TiWi module prior to making a design decision. We know of at least one situation where the TXB type worked for 1 wire SDIO on the TiWi module, but would not work in the 4 wire mode. 1 wire mode uses the TiWi SDIO I/O without the pull ups! Perhaps there is a very weak parasitic pull up within the WL1271 and/or TXB, but we do not recommend using TXB without careful consideration to the logic thresholds.

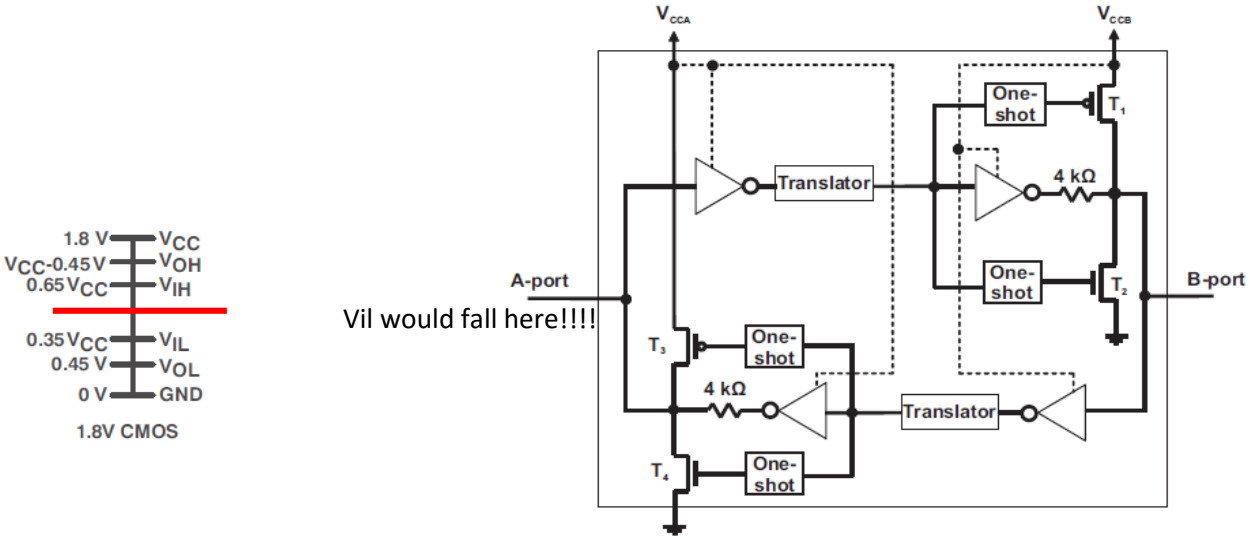
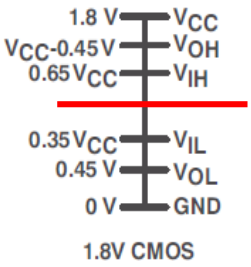



**Figure 5 Texas Instruments TXB010x Voltage Translator**

## 3.2 Maxim MAX13013/MAX13014/MAX3023 Voltage Translators

Below is a snapshot of the architecture of the Maxim MAX13013/MAX13014/MAX3023 single-/dual-/quad-level voltage translators. The simplified architecture shown in Figure 6 is remarkably similar to the TXB series level shifters shown in Figure 5 which were determined to be not a good choice for interfacing with the TiWi module SDIO.




Vil would fall here!!!

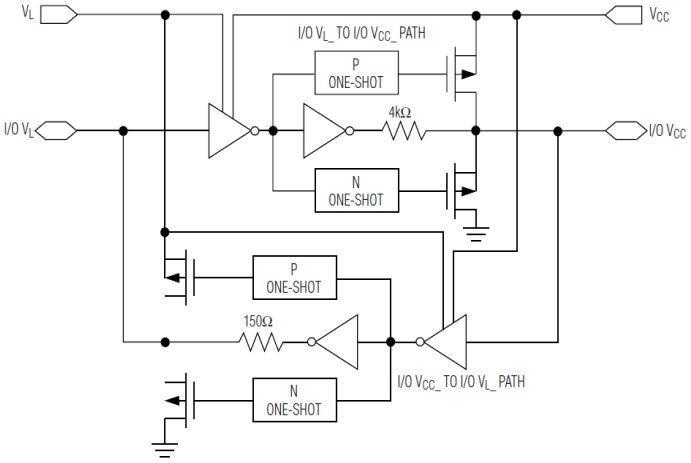



**Figure 6 Maxim MAX13013/MAX13014/MAX3023 Voltage Translator**

## 3.3 Texas Instruments TXS010x Type Voltage Translators

Below is a snapshot of the architecture of the Texas Instruments TXS010x type voltage translators. Again, the SDIO signal to be level translated passes between the A and B ports, and both ports have an internal pull up resistance so this type of translator can pull SDIO lines high for the TiWi module. When a signal with a rising edge is presented to Port A or B, the appropriate one-shot fires briefly for edge acceleration, then the 10K Ω takes over. SDIO_D3 already has a pull up inside the TiWi module, so the 10K Ω will act in parallel with TiWi's 3.21K Ω. For falling edges and logic low, the N2 pass gate is turned on, and the level shifter becomes somewhat transparent. Port A and B are then connected through the pass gate series resistance which is low. Since all SDIO lines except for D3 require an external pull up resistance, this is a good global choice to consider for all of TiWi's SDIO lines. **However, detailed analysis with the SDIO Host must be carried out to ensure logic thresholds are not violated.**

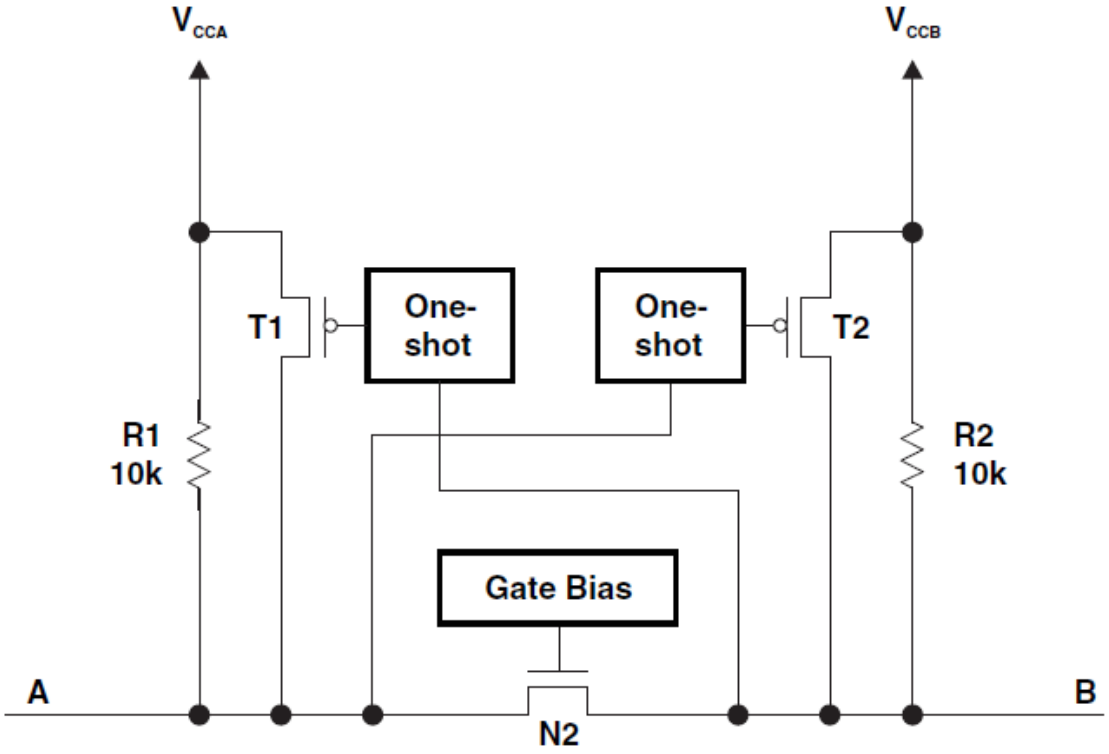



**Figure 7 Texas Instruments TXS010x Voltage Translator**

## 3.4 Texas Instruments TWL1200 Voltage Translator

A noteworthy option to consider is Texas Instrument's TWL1200 which provides 19 bits of voltage translation and is specifically designed to seamlessly bridge TiWi-R2 and TiWi5 modules to application processors operating at different voltages. This translator accommodates voltages from 1.1V to 3.6V. This one part can translate all of TiWi's I/O for approximately $2.00.

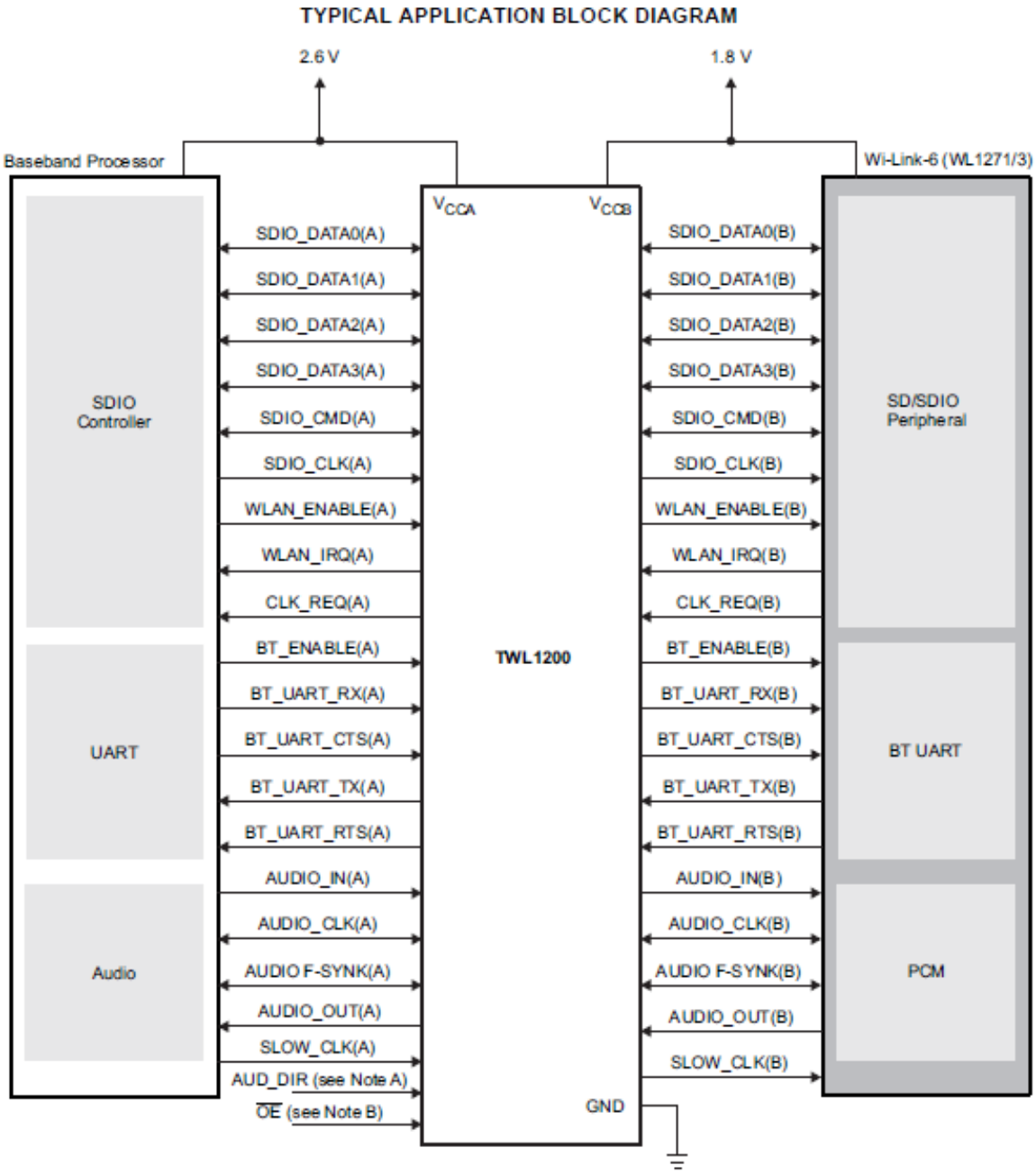



**Figure 8 Texas Instruments TWL1200 Voltage Translator**

# 4 SDIO Level Shifter Conclusions

1. All digital I/O on the TiWi module including the 6 SDIO interface lines require 1.8V logic signals.
2. There is no one size fits all answer to voltage level translation, and when choosing a level shifter or determining if one is required we must pay attention to the requirements of both ends of a SDIO bus
3. There are excellent options readily available to solve each unique set of problems (size, cost, characteristics of your particular host). Keep in mind that choosing a level shifter in a fine pitch BGA package may require fine pitch routing on your host PCB and/or blind vias which will significantly impact the cost of your board.
4. The circuit warrants detailed analysis to ensure logic thresholds are not violated.
5. High speed design techniques should be used as appropriate on the SDIO lines to maintain signal integrity of the rising and falling edges without overshoot or ringing. This is applicable to all digital lines since in addition to helping meet your product performance goals will reduce radiated emissions. These techniques include but are not limited to
    1. Impedance control of the SDIO lines as close to 50 Ω as is practical.
    2. Observing integrity of the ground return paths.
    3. Avoid edge coupling on all SDIO lines.
    4. Consider adding place holders for series resistance on all SDIO lines to suppress ringing. Zero Ω or some small value may be used initially, but then increased to perhaps 33 Ω to suppress ringing if encountered.
    5. Terminating the lines in their characteristic impedance.
6. While the parts recommended in this report are exclusively from Texas Instruments, consideration should be given to other suppliers. The same analysis guidance applies.
7. Please review the application schematic in section 5 & 6 of this document.
8. These notes apply to TiWi-R2, TiWi-BLE and TiWi5.

# 5 TiWi-R2 & TiWi-BLE Recommendations

## 5.1 Vbat and Vio Power Supply Decoupling

The reference schematic in Figure 9 TiWi-R2 & BLE Reference Schematicspecifies the use of particular Johanson capacitors and inductors. We suggest those particular parts be used in the specified packages. The use of these parts is not absolutely required for radiated emission compliance, however, their use will guarantee more margin in the compliance measurements.

| Reference | Value | Manufacturer | Part Number | Description |
|---|---|---|---|---|
| L1 L2 L3 | 2.7nH | Johanson | L-07C2N7SV6T | 0402 SIZE SMT CERAMIC INDUCTOR |
| C1 C2 | 0.50pF | Johanson | 250R05L0R5AV4 | 0201 SIZE SMT CERAMIC CAPACITOR |
| | | Johanson | 250R05L0R5BV4 | |
| | | Johanson | 250R05L0R5CV4 | |

**Table 2 TiWi-R2 & TiWi-BLE Power Supply Decoupling Components**

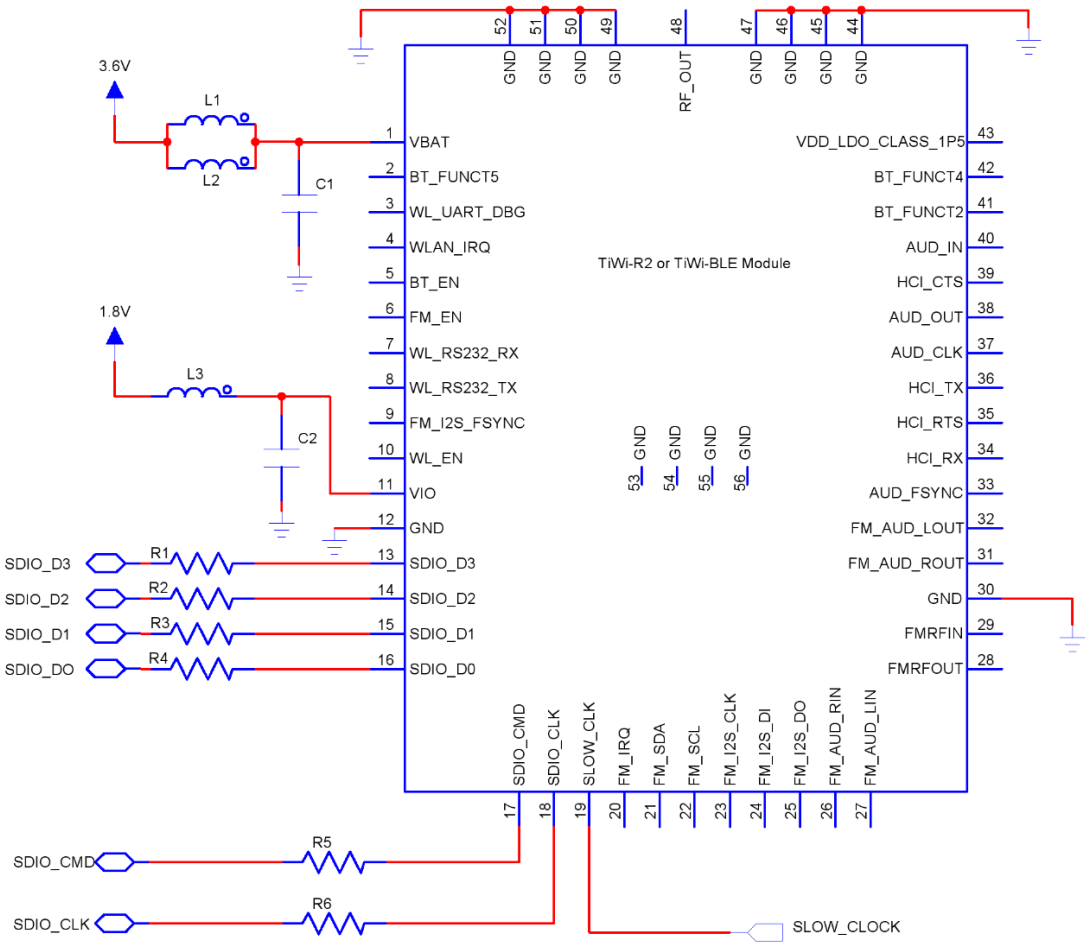


**Figure 9 TiWi-R2 & BLE Reference Schematic**

## 5.2 SDIO and Slow Clock Notes

1. Match electrical length of all 6 SDIO lines.
2. R1 through R6 may be used to suppress ringing on SDIO Lines. Consider using 0 Ω initially and increase values if needed.
3. Target 50 Ω line impedance for all SDIO lines. Verify GND path in final layout.
4. Minimize crosstalk between SDIO lines by leaving GND strips between SDIO signal traces and tie the strips to a ground plane with several vias.
5. All of the modules digital I/O lines are 1.8V logic level. Level shifters must be used if host logic levels are not 1.8V.
6. The 32 KHz slow clock only required to initiate boot up and communication with WLAN or BT. It may be shut off any other time or left running continuously as it is a fails safe module input.

## 5.3 Recommended Top Layer Ground Pattern

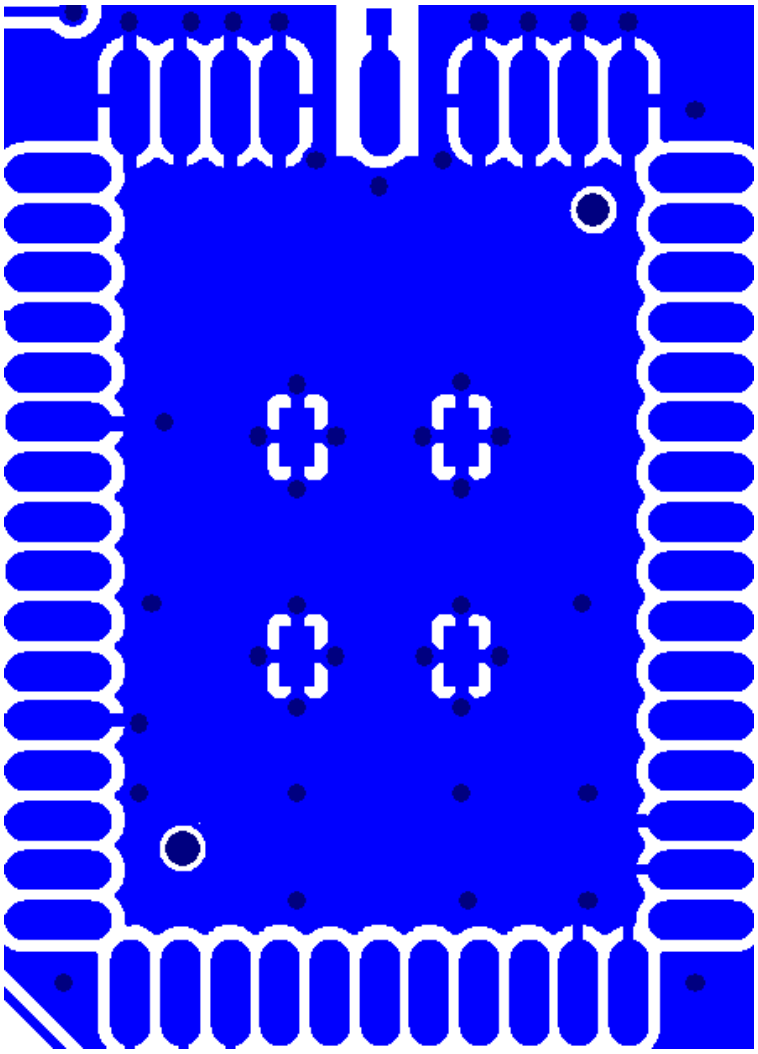


**Figure 10 TiWi-R2 & BLE Recommended Top Layer GND Pattern**

# 6 TiWi5 Recommendations

## 6.1 Vbat and Vio Power Supply Decoupling

The reference schematic in Figure 9 TiWi-R2 & BLE Reference Schematicspecifies the use of particular Johanson capacitors and inductors. We suggest those particular parts be used in the specified packages. The use of these parts is not absolutely required for radiated emission compliance, however, their use will guarantee more margin in the compliance measurements.

| Reference | Value | Manufacturer | Part Number | Description |
|---|---|---|---|---|
| L1 L2 L3 | 1.5nH | Johanson | L-07C1N5SV6T | 0402 SIZE SMT CERAMIC INDUCTOR |
| C1 C2 | 0.30pF | Johanson | 250R05L0R3AV4 | 0201 SIZE SMT CERAMIC CAPACITOR |
| | | Johanson | 250R05L0R3BV4 | |
| | | Johanson | 250R05L0R3CV4 | |

**Table 3 TiWi5 Power Supply Decoupling Components**

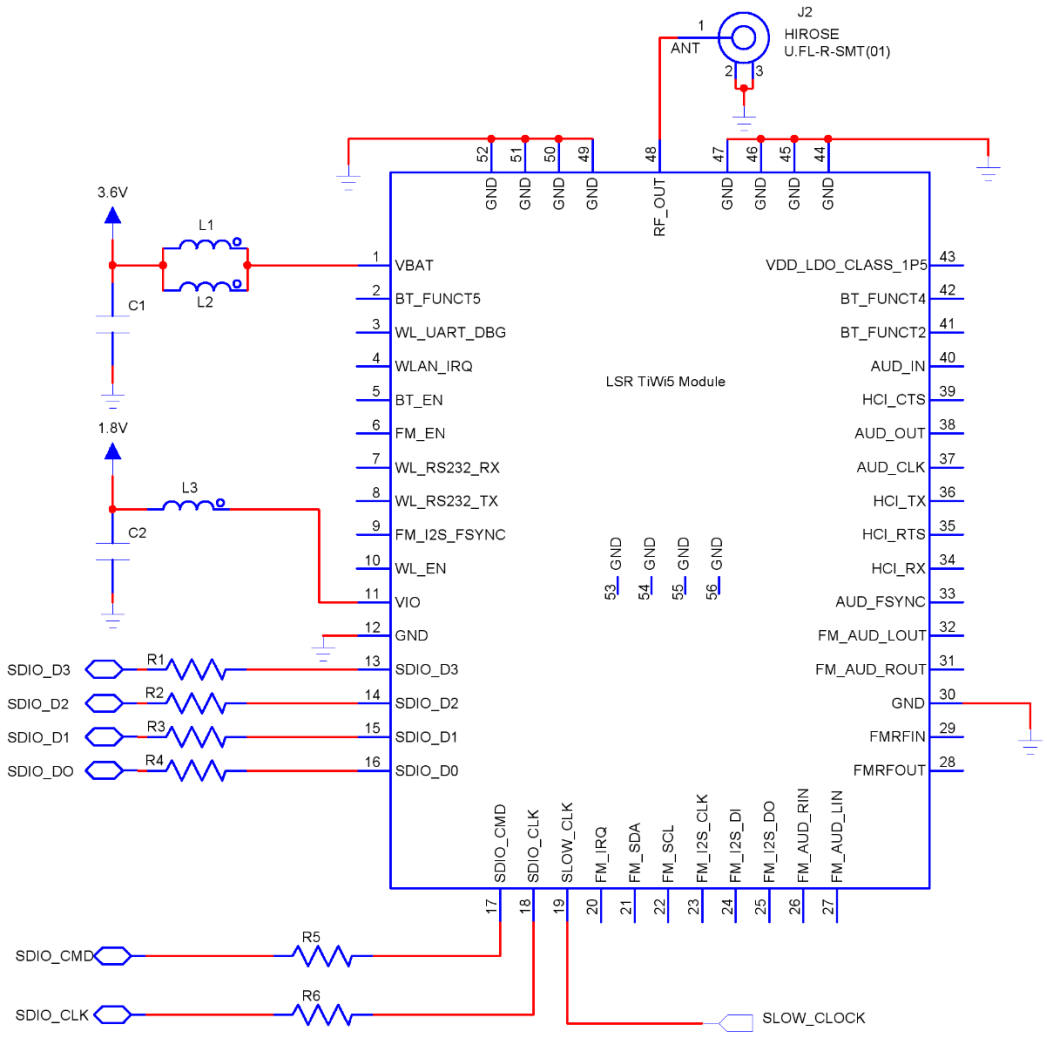


**Figure 11 TiWi5 Reference Schematic**

## 6.2 SDIO and Slow Clock Notes

1. Match electrical length of all 6 SDIO lines.
2. R1 through R6 may be used to suppress ringing on SDIO Lines. Consider using 0 Ω initially and increase values if needed.
3. Target 50 Ω line impedance for all SDIO lines. Verify GND path in final layout.
4. Minimize crosstalk between SDIO lines by leaving GND strips between SDIO signal traces and tie the strips to a ground plane with several vias.
5. All of the modules digital I/O lines are 1.8V logic level. Level shifters must be used if host logic levels are not 1.8V.
6. The 32 KHz slow clock only required to initiate boot up and communication with WLAN or BT. It may be shut off any other time or left running continuously as it is a fails safe module input.

## 6.3 Recommended Top Layer Ground Pattern

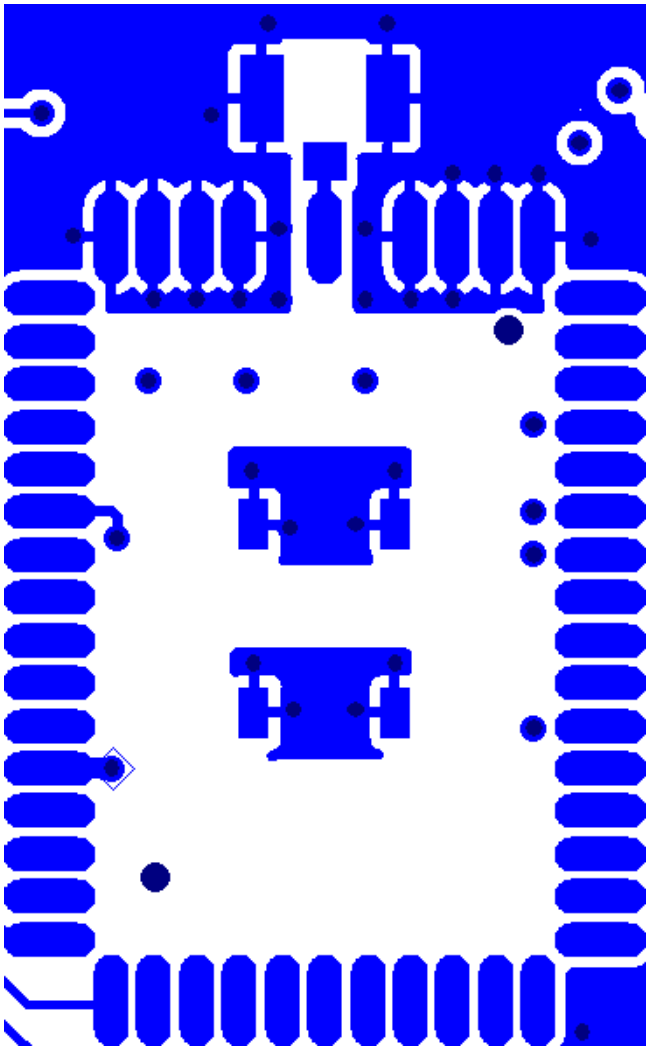


**Figure 12 TiWi5 Recommended Top Layer GND Pattern**

# 7 Contacting LS Research

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