

TIWI FAMILY TRANSCEIVER MODULE

SDIO Interfacing Application Guide



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1 Introduction

1.1 Purpose & Scope

The purpose of this document is to assist in choosing a voltage level translator (aka level shifter, level shifting transceiver), to connect a TiWi family (TiWi or TiWi5) module's 1.8V SDIO to a host system or application processor operating at another voltage. LSR cannot simply provide a list of parts that will work, since the characteristics of the host may be part of the design details required to make a selection. This guide will help the designer analyze the interaction of TiWi module with the level shifter and host such that a choice may be made with confidence.

1.2 Audience

This document is intended to be read by engineers and technical management. A general knowledge of common engineering practices is assumed.

1.3 Applicable Documents

- *TiWi-R2 Datasheet*
- *TiWi5 Datasheet*
- *Texas Instruments Application Report SCEA043*
<http://focus.ti.com/lit/an/scea043/scea043.pdf>
- *Texas Instruments Application Report SCEA044*
<http://focus.ti.com/lit/an/scea044/scea044.pdf>
- *Texas Instruments Voltage Level Translation Selections*
http://focus.ti.com/download/aap/pdf/VLT_PF_Overview.pdf

1.4 Revision History

Date	Change Description	Revision
9-26-2011	Initial release.	1.0

Table 1 Revision History

2 Summary of the Problem - Two Types of SDIO I/O

2.1 SDIO_D3

SDIO_D3 does not require a SDIO Controller (or level shifter) capable of pulling the line high for TiWi. Within the TiWi module, SDIO_D3 is equipped with approximately a 3.21k ohm pull up resistance, while all other SDIO I/O are not pulled up.

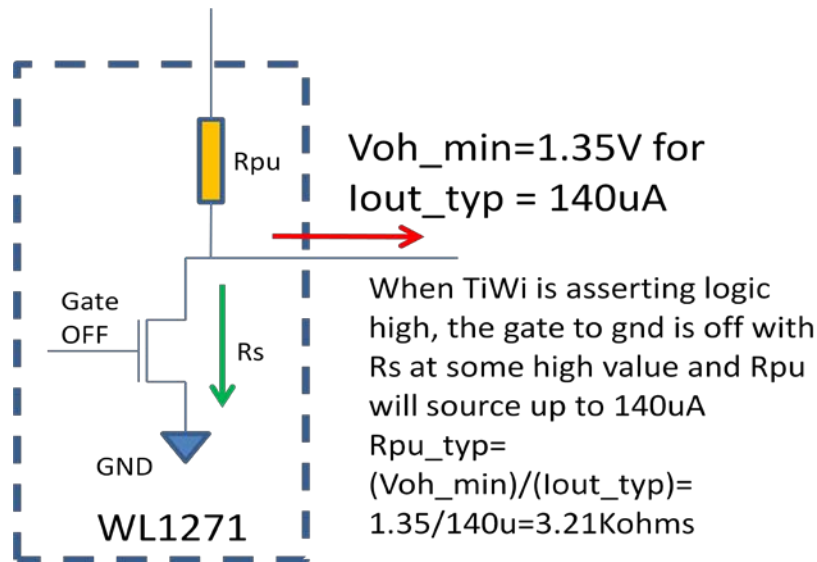


Figure 1 - Logic High: TiWi SDIO_D3

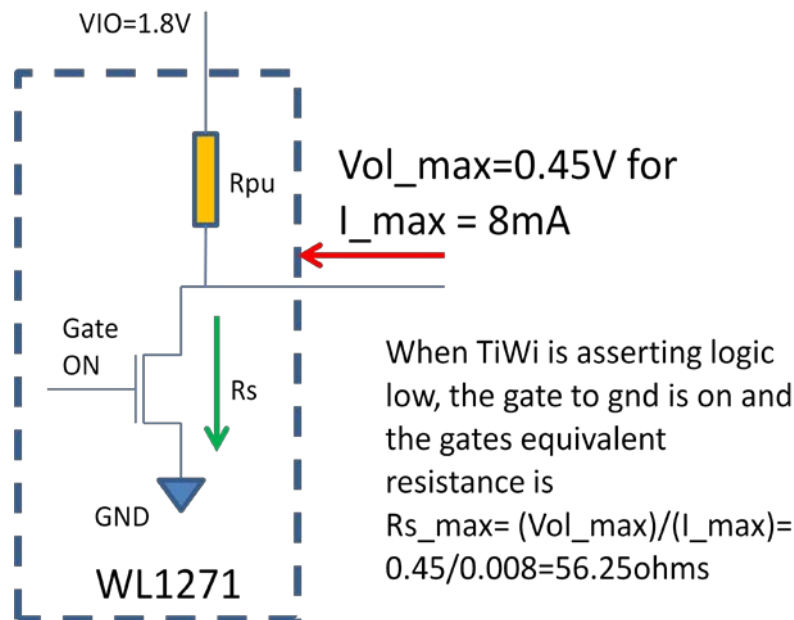


Figure 2 - Logic Low: TiWi SDIO_D3



2.2 All SDIO I/O Except SDIO_D3

All of the SDIO I/O, except SDIO_D3, require a SDIO Controller (or level shifter) capable of pulling the line high for TiWi. An external pull up resistor may be used, but the particular circuit would require detailed analysis to choose the correct value without violating the logic voltage thresholds. The added resistor or network would need to support the data rates and analog rise and fall time of the SDIO bus.

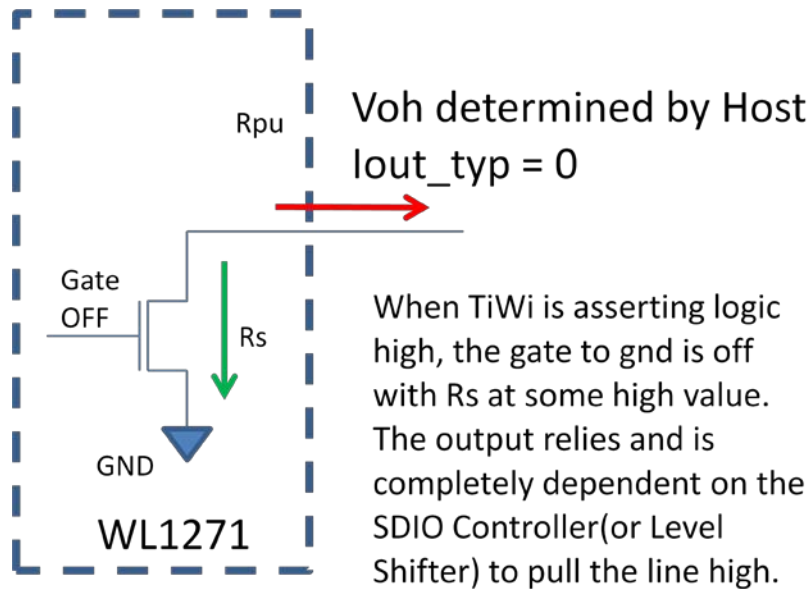


Figure 3 - Logic High: All TiWi SDIO Except SDIO_D3 (open drain requires pull up)

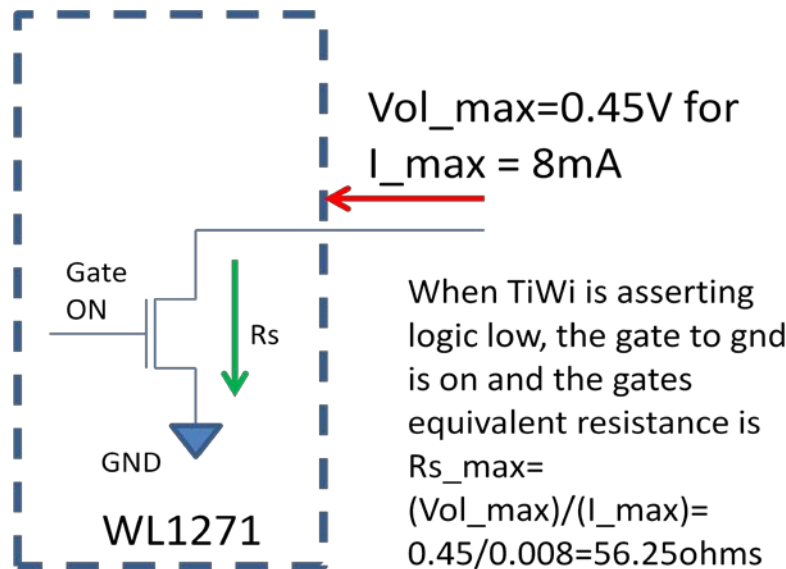


Figure 4 - Logic Low: All TiWi SDIO Except SDIO_D3 (open drain requires pull up)

3 Solutions to Consider

3.1 Texas Instruments TXB010x Type Voltage Translators

Below is a snapshot of the architecture of the Texas Instruments TXB010x type voltage translators. Notice the SDIO signal to be level translated passes between the A and B ports, and neither port has an internal pull up resistance. Since all SDIO lines except for D3 require an external pull up resistance, this is an option only for SDIO_D3 which already has the pull up inside the TiWi module. The appropriate one-shot fires briefly for edge acceleration, then the buffer with series 4K ohms takes over. This would likely not work since when driving a logic low, the 4Kohms is in series with the 3.21K ohms within the TiWi module. This voltage divider results in 0.99 V presented to the TiWi module as a logic low. While this does not meet TiWi's V_{il_max} requirement of 0.63V, we are close and considering the silicon process variation, **this would work intermittently at best, but likely not at all.** It may work with an external pull up network, but there are other choices which will work for all SDIO lines including D3. We suggest detailed analysis of the capabilities of the SDIO Master (or level shifter) and how it relates to and is affected by the TiWi module prior to making a design decision. We know of at least one situation where the TXB type worked for 1 wire SDIO on the TiWi module, but would not work in the 4 wire mode. 1 wire mode uses the TiWi SDIO I/O without the pull ups! Perhaps there is a very weak parasitic pull up within the WL1271 and/or TXB, but we do not recommend using TXB without careful consideration to the logic thresholds.

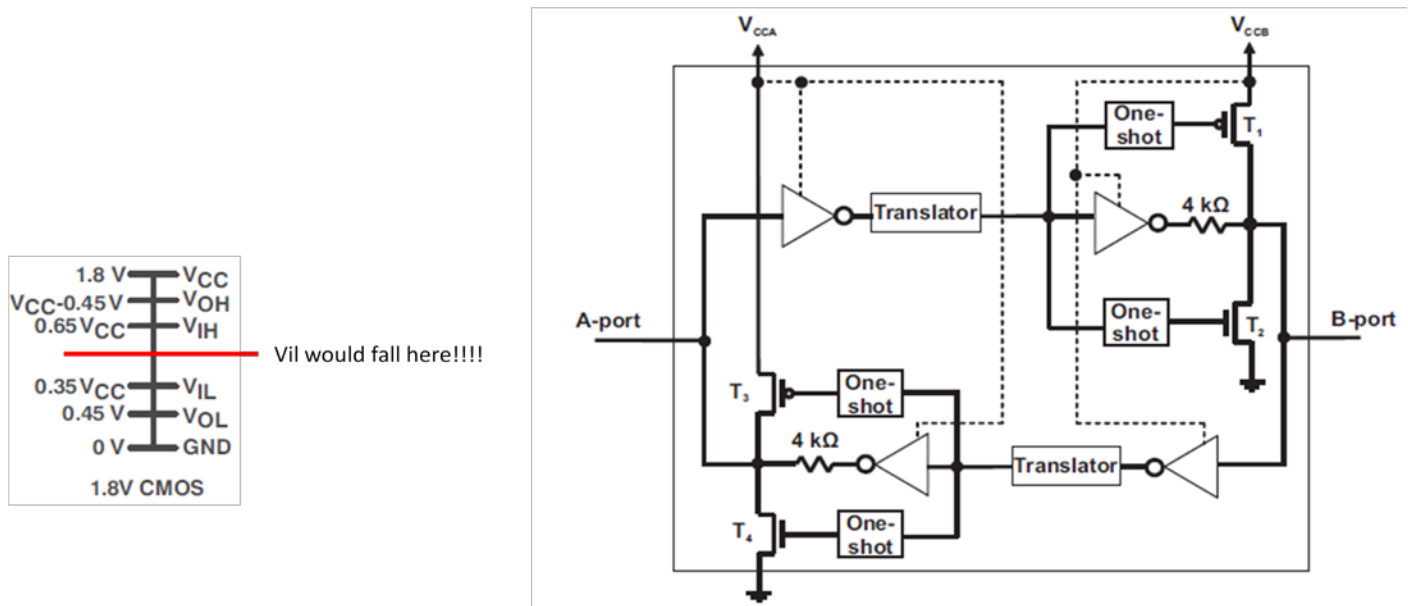


Figure 5 – Texas Instruments TXB010x Voltage Translator



3.2 Texas Instruments TXB010x Type Voltage Translators

Below is a snapshot of the architecture of the Texas Instruments TXS010x type voltage translators. Again, the SDIO signal to be level translated passes between the AA and B ports, and both ports have an internal pull up resistance so this type of translator can pull SDIO lines high for the TiWi module. When a signal with a rising edge is presented to Port A or B, the appropriate one-shot fires briefly for edge acceleration, then the 10K ohms takes over. SDIO_D3 already has a pull up inside the TiWi module, so the 10K ohms will act in parallel with TiWi's 3.21K ohms. For falling edges and logic low, the N2 pass gate is turned on, and the level shifter becomes somewhat transparent. Port A and B are then connected through the pass gate series resistance which is low. Since all SDIO lines except for D3 require an external pull up resistance, this is a good global choice to consider for all of TiWi's SDIO lines. **However, detailed analysis with the SDIO Host must be carried out to ensure logic thresholds are not violated.**

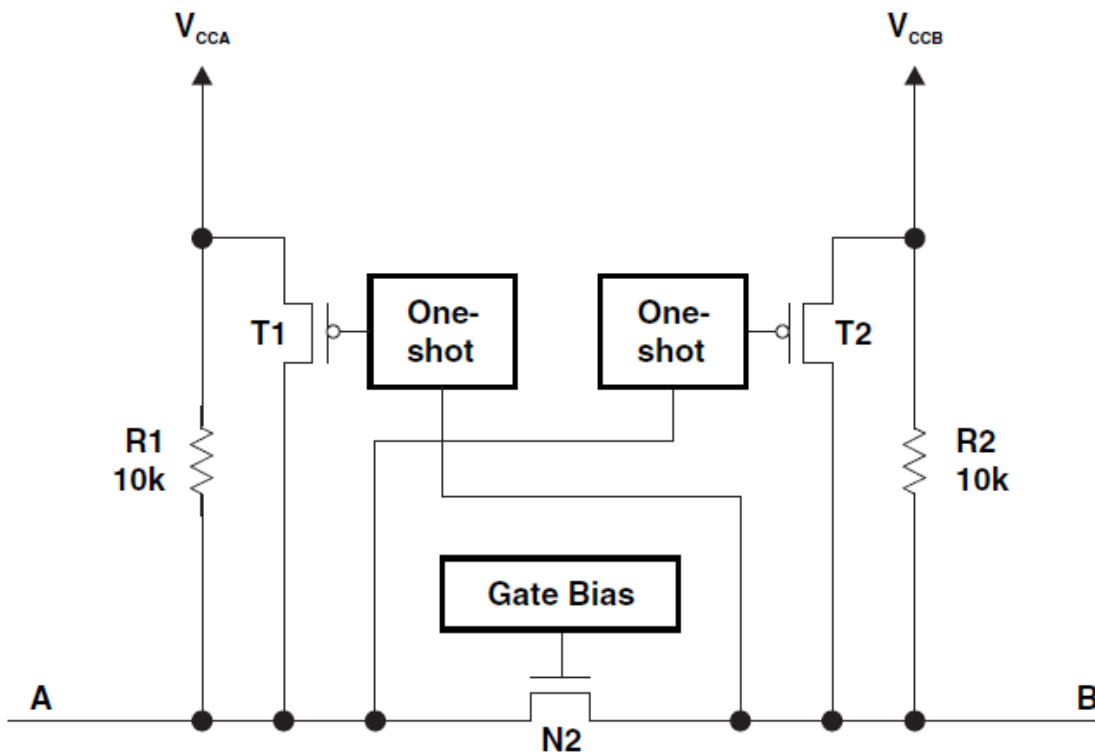


Figure 6 – Texas Instruments TXS010x Voltage Translator



3.3 Texas Instruments TWL1200 Voltage Translator

A noteworthy option to consider is Texas Instrument's TWL1200 which provides 19 bits of voltage translation and is specifically designed to seamlessly bridge TiWi-R2 and TiWi5 modules to application processors operating at different voltages. This translator accommodates voltages from 1.1V to 3.6V. This one part can translate all of TiWi's I/O for approximately \$2.00.

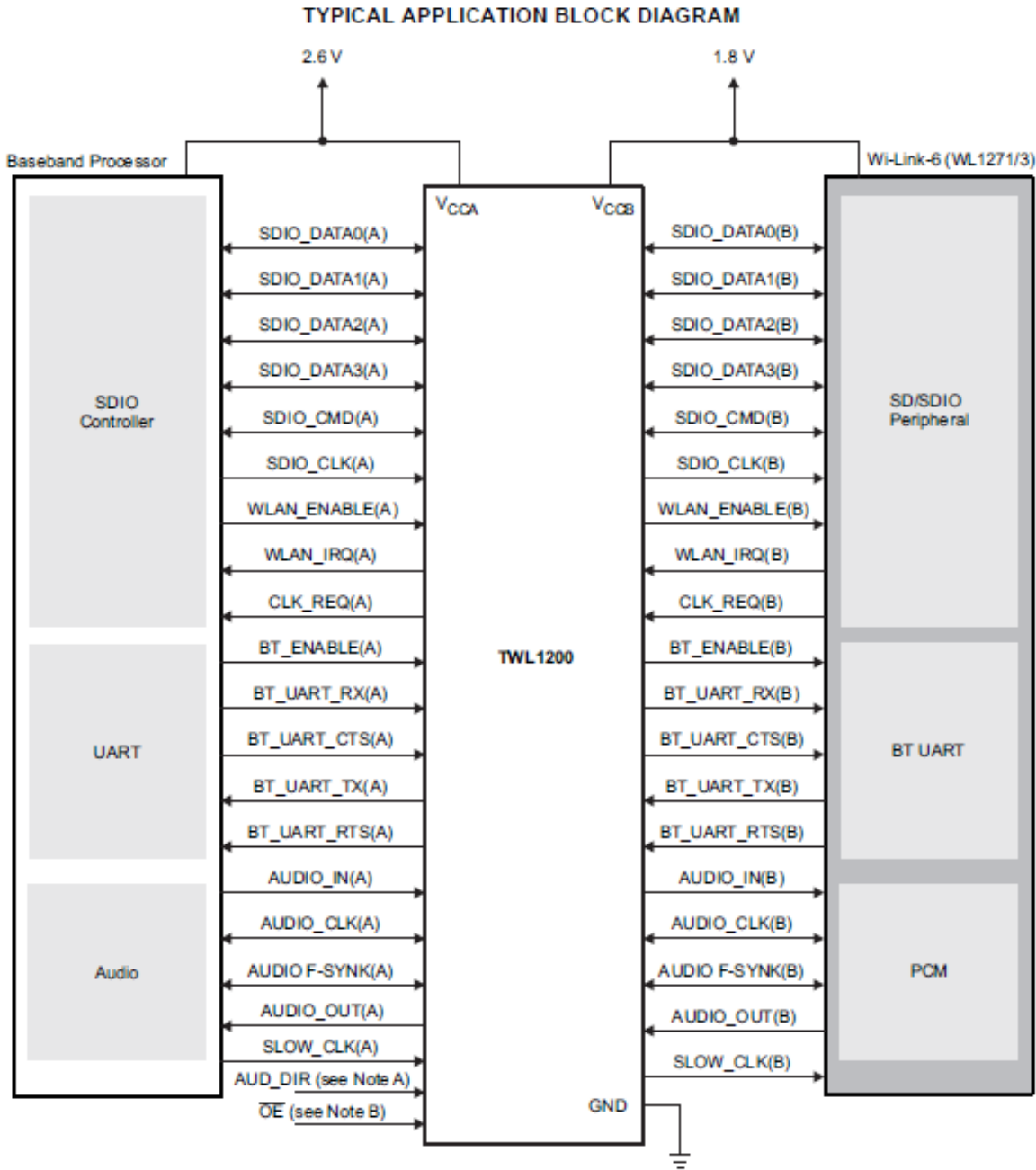


Figure 7 – Texas Instruments TWL1200 Voltage Translator

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4 Conclusions

1. There is no one size fits all answer to voltage level translation.
2. There are excellent options readily available to solve each unique set of problems (size, cost, characteristics of your particular host).
3. The circuit warrants detailed analysis to ensure logic thresholds are not violated.
4. High speed design techniques should be used as appropriate for the rise and fall times and data rates to be supported. This is always true for all digital lines, and in addition to helping meet your product performance goals will reduce radiated emissions. These techniques include but are not limited to
 1. Impedance control of the SDIO lines.
 2. Observing integrity of the ground return paths.
 3. Consider adding place holders for series resistance on all SDIO lines to suppress ringing. Zero ohms or some small value may be used initially, but then increased to perhaps 33 ohms to suppress ringing if encountered.
 4. Terminating the lines in their characteristic impedance.
5. While the parts considered in this report were all from Texas Instruments, consideration should be given to other suppliers. The same analysis guidance applies.

5 Contacting LS Research

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